REMARKS

By the present response, Applicant has amended claims 2, 5, 9, 10, 16, 18, 19, 22-25 and 27 to further clarify the invention. Claims 1-27 are pending in this application. Reconsideration and withdrawal of the outstanding rejections and allowance of the present application are respectfully requested in view of the above amendments and the following remarks.

In the Office Action, claims 1-27 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,813,721 (Tetreault et al.) and "MPC8xx SDRAM Interface"-11/2001 (Wrobel).

35 U.S.C. § 103 Rejections

Claims 1-27 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Tetreault et al. in view of Wrobel. Applicant respectfully traverses these rejections.

Tetreault et al. discloses maintaining clock phase alignment among system modules of a fault–computing system. A low-frequency system reference clock signal is distributed to all system modules where it is multiplied to generate higher-frequency local clock signals. All local clock signals are then synchronized to the rising edge of the reference clock signal and the first rising edge in relation to a timely event is also identified.

Wrobel discloses a design concept where the basis of SDRAM operation is discussed as well as an illustration of a method of interfacing SDRAM to the MPC8xx processor. A general procedure to interface the SDRAM is described as well as associated issues.

Regarding claims 1, 19, 18, 22 and 25, Applicant submits that none of the cited references, taken alone or in any proper combination, disclose suggest or render obvious the limitations in the combination of each of these claims. For example, the Examiner asserts that Tetreault et al. discloses a first device operated according to a first clock and generating control signals at a speed of a second clock, at col. 2, lines 65-col. 3, line 3. However, these portions merely disclose that each processor in a CPU or I/O module, contains a local clock generator that receives the distributed reference clock signal and generates a respective local clock signal from this system reference clock signal. This is not a first device operated according to a first clock signal and generating control signals at a speed of a second clock, as recited in the claims of the present application. These portions merely relate to generating higher frequency local clock signals based on a low-frequency reference clock signal. These portions do not disclose or suggest anything related to generating control signals.

The Examiner further asserts that Tetreault et al. discloses a second device operated by being synchronized with the second clock according to the control signals, at col. 3, lines 6-10. However, these portions merely disclose that a zero clock detector may exist in each of the processors or may be common on a CPU to all processors, where the zero clock detector identifies a particular clock cycle. This is not a second device operated by being synchronized with the second clock according to the control signals and having an operation latency of one clock period of the first clock, as recited in the claims of the present application. These portions

merely relate to potential locations of the zero clock detector. These portions do not disclose or suggest anything related to a second device being synchronized with a second clock according to control signals, or an operation latency of one clock period of the first clock.

The Examiner further asserts that Tetreault et al. discloses a clock driver generating the second clock by multiplying the first clock by predetermined even times and removing a phase delay between the second clock and the first clock, at col. 6, lines 35-37 and col. 3, lines 43-53. However, these portions merely disclose that the local clock signal may be input into a driver for distribution to other circuits, and that the added time delay due to the driver may be compensated for by use of a zero-delay-buffer PLL. These portions disclose compensating for delays added in the distribution of the local clock signal. This is not removing a phase delay between the second clock and the first clock, as recited in the claims of the present application.

Moreover, none of the cited references disclose or suggest programming a generation interval of random access memory control signals so as to correspond to an operation latency of a RAM that interfaces with a microprocessor having a speed of predetermined even times a speed of a microprocessor clock, or generating the RAM control signals corresponding to a specific operation mode at a speed of a RAM clock according to the programmed generation interval and outputting the RAM control signals from the microprocessor to the RAM, or performing a read operation of a microprocessor according to a clock suspension function of a random access memory, or outputting a clock enable signal from the microprocessor according

to a clock suspension function of the RAM. The Examiner provides no portion of any references that disclose or suggest these limitations in the claims of the present application.

In addition, Applicant submits that one of ordinary skill in the art would have no motivation to combine Tetreault et al. that relates to maintaining clock phase alignment by using a low frequency clock to generate higher frequency local clock signals with Wrobel that simply relates to a design concept for interfacing SDRAM to a very specific line of processors, namely MPC8xx processors. Further, this combination fails to achieve the limitations in the claims of the present application.

Regarding claims 2-8, 10-17, 19-21, 23, 24, 26 and 27, Applicant submits that these claims are dependent on one of independent claims 1, 9, 18, 22 and 25 and, therefore, are patentable at least for the same reasons noted previously regarding these independent claims.

Accordingly, Applicant submits that none of the cited references, taken alone or in any proper combination, disclose suggest or render obvious the limitations in the combination of each of claims 1-27 of the present application. Applicant respectfully requests that these rejections be withdrawn and that these claims be allowed.

CONCLUSION

In view of the foregoing amendments and remarks, Applicant submits that claims 1-21 are now in condition for allowance. Accordingly, early allowance of such claims is respectfully requested. If the Examiner believes that any additional changes would place the application in better condition for allowance, the Examiner is invited to contact the undersigned attorney, Frederick D. Bailey, at the telephone number listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this, concurrent and future replies, including extension of time fees, to Deposit Account 16-0607 and please credit any excess fees to such deposit account.

Respectfully submitted,
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